CLAIMS

1. A multiband PLL arrangement comprising a single loop PLL with a phase/frequency detecting means (1), a loop filter means (2) and a Voltage Controlled Oscillator (VCO) (3), to which PLL a reference voltage signal ($V_{ref}$) is input,
c h a r a c t e r i z e d i n
that it further comprises a control circuit for appropriately locking the VCO (3) to the correct frequency band, said control circuit comprising a multi-window circuit (4) with at least first and second window amplitudes each defined by respective upper and lower voltage levels, and in that comparing means (5A, 5B) are provided for comparing a first VCO control voltage output from the loop filter means (2) with the upper and lower voltage levels of a first, broadest amplitude window, and in that if the VCO control voltage settles within said first amplitude window, a narrower window is selected, the voltage levels of which are compared with the VCO control voltage and in that if the VCO control voltage settles within that or a further subsequent, smaller amplitude window, phase lock is achieved, otherwise, if the VCO control voltage does not settle within said windows, this is established by the comparing means (5A, 5B), said comparing means (5A, 5B) providing a signal for providing a second control signal to the VCO (3) for switching it to another, higher or lower, frequency band, and in that for said other frequency band, the resulting first VCO control voltage signal is compared with said first amplitude window etc. until phase lock is achieved in the appropriate frequency band.

2. An arrangement according to claim 1,
c h a r a c t e r i z e d i n
that the first VCO control voltage comprises an analog signal.

3. An arrangement according to claim 2,
c h a r a c t e r i z e d i n
that the second VCO control signal is digital.

4. An arrangement according to claim 3,
c h a r a c t e r i z e d i n
that the comparing means comprises a first and a second comparator (5A, 5B) for comprising the first VCO control voltage with the upper voltage level and the lower voltage level respectively, and in that if the first VCO control voltage exceeds the upper voltage level or falls below the lower voltage level, a corresponding signal is provided to switching enabling means (7) to indicate whether a switch is to be done to a higher or a lower frequency band.

5. An arrangement according to any one of claims 1-4,
c h a r a c t e r i z e d i n
that the comparing means (5A, 5B) are connected to first delay means (6) such that if a switching is required to another frequency band, the appropriate signal is clocked into the switching enabling means (7) after lapse of a given time period.

6. An arrangement according to claim 5,
c h a r a c t e r i z e d i n
that the switching enabling means comprises a state machine (7) which upon reception of the clocked signal from the comparing means (5A, 5B) provides the second control signal to the VCO (3), enabling a shift in frequency band.

7. An arrangement according to any one of the preceding claims,
c h a r a c t e r i z e d i n

that when phase lock has been achieved, an arbitrary operating window size can be selected among the window sizes available in the multi-window circuit (4).

8. An arrangement according to any one of the preceding claims,
c h a r a c t e r i z e d i n
that the control circuit comprises a lock detection circuit (12) for (continuously) monitoring whether phase lock has been achieved.

9. An arrangement according to claim 8,
c h a r a c t e r i z e d i n
that the lock detection circuit (12) comprises means for initializing restart of the locking procedure if locking has failed or if lock is lost.

10. An arrangement according to claim 9,
c h a r a c t e r i z e d i n
that the lock detection circuit (12) uses signals output from the comparators (5A, 5B) and from the multi-window circuit (4) to establish if the first VCO control voltage falls within the relevant amplitude window or not, such that if the first VCO control voltage falls outside the amplitude window, the locking procedure is restarted, otherwise a lock achieved condition is indicated.

11. An arrangement according to any one of the preceding claims,
c h a r a c t e r i z e d i n
that it comprises a loop switch arrangement, comprising a threshold circuit (8), for adjusting the VCO control voltage to

substantially assume a desired voltage within the relevant amplitude window after band switching.

12. An arrangement according to claim 11,
c h a r a c t e r i z e d i n
that the threshold circuit (8) controls a switching arrangement comprising two transistors (9A, 9B) for, depending on whether an adjustment upwards or downwards of the voltage is required, charging/discharging a VCO control voltage control point (CP) using the supply voltage/ground until the VCO control voltage substantially assumes the desired voltage within the amplitude window.

13. An arrangement according to claim 12,
c h a r a c t e r i z e d i n
that to the threshold circuit (8) signals are input from the first and second comparators (5A, 5B) and the analog VCO control signal, and in that the threshold circuit (8) uses the input signals to establish whether an adjustment upwards or downwards of the analog VCO control signal is needed, or if no adjustment is needed.

14. An arrangement according to any one of the preceding claims,
c h a r a c t e r i z e d i n
that a single supply voltage is used.

15. An arrangement according to anyone of the preceding claims,
c h a r a c t e r i z e d i n
that the PLL is a narrowband PLL.

16. An arrangement at least according to claim 7,
c h a r a c t e r i z e d i n

that upon completed phase lock, an amplitude window at least somewhat larger than the smallest amplitude window within which phase lock was accomplished, is selected as operation window.

17. An arrangement at least according to claim 12, c h a r a c t e r i z e d i n that the control point (CP) is located in the loop filter means (2).

18. An arrangement according to claim 17, c h a r a c t e r i z e d i n that the loop filter (2) is an active filter comprising an amplifier (A) and in that the control point (CP) is located before the amplifier (A).

19. An arrangement according to any one of claims 1-16, c h a r a c t e r i z e d i n that it comprises a charge pump PLL and in that the loop filter means are comprised in the charge pump, the filter being a passive filter, a charge storing means of which being charged/discharged for VCO control voltage controlling purposes.

20. A method for controlling a multiband arrangement comprising a single loop PLL with a phase/frquency detector, a loop filter means and a Voltage Controlled Oscillator, wherein a reference voltage signal ($V_{ref}$) is input to the arrangement, c h a r a c t e r i z e d i n that it comprises the steps of:

- providing the reference voltage $V_{ref}$ signal at least to a PLL comprising a phase/frequency detector and a loop filter means and to a multi-window circuit;

- setting a first, large, amplitude window defined by an upper and a lower voltage level in the multi-window circuit;
- establishing whether the first analog VCO control voltage output from the low-pass filter settles within the first amplitude window, if yes, changing the multi-window circuit to a smaller amplitude window at least once; while
- establishing if the first VCO control voltage settles within the voltage amplitude interval of the smaller window; if not,
- using the result of the comparison to establish whether a switch to a higher or a lower frequency band should be done;
- providing a digital control signal to the VCO to switch it to such higher or lower frequency band;
- repeating the procedure by first implementing a large amplitude interval, followed by at least one smaller window unless a further frequency band switch is required etc. until phase lock is achieved within the appropriate frequency band.

21. A method according to claim 20,
characterized in
that it comprises the step of:
- resetting the VCO control voltage when there is a switch of frequency band.

22. A method according to claim 20 or 21,
characterized in
that it comprises the step of:
- adjusting the VCO control voltage after switching frequency band to make it assume a desired voltage within the amplitude window by means of a digital threshold circuit

and a transistor arrangement and using a single supply voltage.

23. A method according to any one of claims 20-22, characterized in that it comprises the steps of:
- continuously monitoring whether a lock condition has been achieved, and
- indicating when lock has been achieved, e.g. by establishing that lock has been achieved in the smallest window, or
- initiating a restart of the locking procedure if a switching of frequency band is needed, i.e. if the control voltage does not settle within an amplitude window.

24. A method at least according to claim 21, characterized in that it comprises the step of:
- providing a signal from the transistor arrangement to a control point (CP) in the loop filter.

25. A method according to claim 22, characterized in that the loop filter is an active filter.

26. A method according to claim 25, characterized in that said control point (CP) is located before the loop filter amplifier.

27. A method according to any one of claims 20-24, characterized in

that the arrangement comprises a phase frequency detector and a charge pump comprising the loop filter functionality.

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